REMARKS

Claims 1, 4, and 18 have been amended. Claims 1-20 remain pending in the present application and are presented to the Examiner for consideration in light of the amendments and remarks made herein.

The Examiner rejected claims 1-3 under 35 U.S.C. §102(a) as being anticipated by Ker (U.S. Patent No. 5,901,022). Applicants respectfully traverse this rejection.

In the rejection, the Examiner alleges that Ker discloses an ESD circuit having an inductor connected to a plurality of ESD clamp devices. The Examiner further alleges that Ker discloses in Figures 11 and 12 that the inductor is formed on a substrate (die). Applicants, however, respectfully disagree with the Examiner's interpretation of Ker.

Although Ker may disclose an electrostatic discharge (ESD) protection circuit, it is noted that the invention of Ker (in the various embodiments illustrated in Figures 9-12) includes a single coil and a single ESD clamp device. It is respectfully submitted, however, that independent claim 1 of the present invention (as amended) recites "an inductor having a plurality of turns in the shape of a coil" and "a plurality of electrostatic discharge (ESD) clamp devices." Although the Examiner alleges that Ker provides more than one ESD clamp device (although this is not apparent from Figures 9-12 which clearly show only one ESD clamp device), independent claim 1 has been amended to indicate that the plurality of ESD clamp devices are connected *to a corresponding one of* the plurality of turns of the inductor. Applicants respectfully submit that Ker does not teach or suggest a plurality of ESD clamp devices that are connected to a corresponding one of the plurality of turns of the inductor as defined by claim 1 of

the present invention. Accordingly, because Ker fails to teach providing a plurality of ESD clamp devices being connected to a corresponding one of the plurality of turns of an inductor in an ESD protection network, Ker cannot possibly anticipate claim 1 of the present invention (as amended), and claims 2 and 3 that depend thereon.

The Examiner further rejected claim 1 under 35 U.S.C. §102(a) as being anticipated by Japanese Patent Abstract JP-67486 (hereinafter "the Japanese reference"). Applicants respectfully traverse this rejection.

Although the Japanese reference cited by the Examiner may disclose an ESD protection circuit, Applicant respectfully submits that the reference fails to teach or suggest using more than one ESD clamp device that are connected to a corresponding one of a plurality of turns of an inductor in an ESD protection network. As previously mentioned, claim 1 of the present invention (as amended) includes a plurality of ESD clamp devices connected to a corresponding one of a plurality of turns of an inductor. Accordingly, because the Japanese reference fails to teach the use of more than on ESD clamp device within an ESD protection network being connected to a corresponding one of a plurality of turns of an inductor, it is respectfully submitted that the Examiner's allegation that the Japanese reference anticipates claim 1 of the present invention is improper.

The Examiner rejected claims 2 and 3 under 35 U.S.C. §103(a) as being unpatentable under Japanese Patent Abstract (JP-67486) in view of Ker. Applicants respectfully traverse this rejection.

In the rejection, the Examiner alleges that the Japanese reference discloses all the features of claim 1 except the inductor being fabricated on a substrate or an IC die. The Examiner relies

on Ker for teaching (in Figures 11 and 12) an inductor being formed on a substrate/die (bond metal pad) to avoid increasing the total layout area of the protection circuit. The Examiner then alleges that it would have been obvious to utilize the teaching of Ker to form the inductor on the bond pad to save space on the integrated circuit. Applicants, however, respectfully disagree with this rejection.

As previously indicated, although the Japanese reference cited by the Examiner may disclose an ESD protection circuit, the reference fails to teach or suggest using more than one ESD clamp device being connected to a corresponding one of a plurality of turns of an inductor. Claim 1 of the present invention (as amended) includes a plurality of ESD clamp devices that are connected to a corresponding one of the turns of an inductor. Accordingly, because the Japanese reference fails to teach the use of more than on ESD clamp device connected to a corresponding one of the turns of an inductor within an ESD protection network, it is respectfully submitted that claims 2 and 3 of the present invention are distinct therefrom. Additionally, although Ker may teach an inductor being formed on a substrate as alleged by the Examiner, Applicant respectfully submits that the ESD circuit of Ker has an inductor coupled to a single ESD clamp device and that there is absolutely no teaching or suggestion provided by Ker to provide more than one ESD clamp connected to a corresponding one of the turns of an inductor. Accordingly, because neither the Japanese reference nor Ker teach to provide a plurality of ESD clamp devices connected to a corresponding one of the turns of an inductor in an ESD protection network, these references cannot possibly make obvious claims 2 and 3 of the present invention.

The Examiner also rejected claims 4-20 under 35 U.S.C. §103(a) as being unpatentable under Ker in view of Lee (U.S. Patent No. 5,831,331). Applicants respectfully traverse this rejection.

In the rejection, the Examiner alleges that Ker discloses an ESD protection circuit connected to an inductor formed on a substrate of an integrated circuit, but fails to disclose the physical structure of the multi-coil turn inductor on a plurality of insulating layers. The Examiner alleges that Lee discloses an integrated circuit inductor having multiple coil turns. The Examiner then alleges that it would have been obvious to utilize the inductive structure taught by Lee in Ker to save space on the integrated circuit and for ease of manufacturing. Applicants respectfully disagree with this rejection.

The Lee reference is directed to an inductor having multiple turns disposed one above another in respective metallization layers of an IC. Although Lee may teach or suggest a "stacked" coil configuration, Lee does not teach or suggest the use of more than one ESD clamp device with the plurality of coils. It is respectfully submitted that a combination of Ker with Lee would teach at most an ESD protection circuit having a plurality of coils stacked upon one another with a single ESD clamp device. Accordingly, it is submitted that Ker and Lee, taken alone or in combination, do not teach or suggest the use of more than one ESD clamp device being connected to a corresponding one of coil turns of a plurality of conductive layers as set forth in independent claims 4 and 18 of the present invention. For example, claim 4 recites "*said plurality of* electrostatic discharge (ESD) clamp devices being connected *to a corresponding one of* the coil turns of said plurality of conductive layers," and claim 18 recites "connecting *said plurality of* ESD clamp devices *to a corresponding one of* the coil turns of said plurality of conductive layers" (emphasis added). Therefore, because the Ker or Lee references, either taken alone or in combination, fail to teach or suggest providing more than one ESD clamp device being connected *to a corresponding one of* the coil turns of said plurality of conductive layers, it

is respectfully submitted that the Examiner's allegation of obviousness in view of the Ker and Lee references is improper.

Applicants respectfully submit that the remaining rejections in the present application are improper and should be withdrawn because the cited references fail to teach or suggest all of the limitations of the claims as discussed in detail above. Accordingly, in view of the amendments and remarks presented herein, a Notice of Allowance is respectfully solicited.

It is believed that no fee is due in connection with filing this paper; however, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be required for any reason, the Assistant Commissioner is authorized to deduct said fees from Williams, Morgan & Amerson, P.C. Deposit Account No. 50-0786/2000.065900.

The Examiner is invited to contact the undersigned at (713) 934-4058 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

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APPENDIX A

1. (Twice Amended) An electrostatic discharge (ESD) protection network, comprising:

an inductor having a plurality of turns in the shape of a coil, the plurality of turns having an inductance; and

a plurality of electrostatic discharge (ESD) clamp devices, each one of said plurality of ESD clamp devices having a parasitic capacitance, said plurality of ESD clamp devices being connected to a corresponding one of said plurality of [the] turns of said inductor, the inductance of said turns and the parasitic capacitance of said ESD clamp devices thereby forming a low pass filter.

4. (Amended) An integrated circuit apparatus having an electrostatic discharge (ESD) protection network, said apparatus comprising:

an integrated circuit substrate;

a first insulation layer over a face of said integrated circuit substrate;

a plurality of conductive layers, each of the plurality of conductive layers in the shape[d] of a coil turn, the coil turn having a first and second end;

a plurality of insulation layers interleaved between the plurality of conductive layers;

a one of said plurality of conductive layers proximate to said first insulation layer and the other ones of said plurality of conductive layers stacked over the one with said plurality of insulation layers interleaved therebetween;

a plurality of vias in the plurality of insulation layers, the plurality of vias connecting adjacent ones of the coil turns of said plurality of conductive layers, thereby forming an inductor coil; and

a plurality of electrostatic discharge (ESD) clamp devices, each one of said plurality of ESD clamp devices having a parasitic capacitance, said plurality of ESD clamp devices being connected to a corresponding one of the [inductor] coil turns of said plurality of conductive layers, thereby forming a low pass filter.

18. (Amended) A method for providing an electrostatic discharge (ESD) protection network, comprising [the steps of]:

forming a plurality of conductive layers and a plurality of insulation layers, wherein said plurality of conductive [of] layers and said plurality of insulation layers are interleaved, wherein each of the conductive layers is formed in the shape[d] of a coil turn [of a coil] having an inductance such that such that each of the coil turns has a first and a second end;

forming a plurality of vias in said plurality of insulation layers, the plurality of vias being located between the ends of adjacent coil turns wherein conductive material is formed in said plurality of vias thereby connecting the first end of one coil turn to the second end of the adjacent coil turn;

providing a plurality of electrostatic discharge (ESD) clamp devices, each one of said plurality of ESD clamp devices having a parasitic capacitance; and

connecting said plurality of ESD clamp devices to a corresponding one of the coil turns of said plurality of conductive layers, thereby forming a low pass filter.